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EXAMINER	
LAMARRE, GUY J	
ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 02/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/752,879	Applicant(s) MUKHERJEE, ADITYA	
	Examiner Guy J. Lamarre, P.E.	Art Unit 2133	

-- Th MAILING DATE of this communication appears on the cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 Nov. 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

FINAL OFFICE ACTION

1. This office action is in response to Applicants' **Amendment** of 25 Nov. 2003. The terminal disclaimer, jointly submitted, has entered.

1.1 **Claims** 1, 3-4, 6-8, 11-13, 16 and **18-19** are amended. **Claims 1-20** remain pending.

1.2 The **prior art** rejections of record are withdrawn in response to Applicants' **Amendment** of 25 Nov. 2003.

1.3 The **non-statutory Double Patenting** rejections of record are withdrawn in response to Applicants' timely filed terminal disclaimer of 25 Nov. 2003.

1.4 The objections of record to the **Claims** are withdrawn in response to Applicants' amendment of **25 Nov. 2003**.

Response to Arguments

2. Applicants' arguments of **25 Nov. 2003** have been fully considered, and are deemed persuasive only to the extent that the newly added limitations or approach whereby 'the ITC having an instruction register and a test access port finite state machine and the tester is embedded into the device under test' is not specifically disclosed in detail by the prior art of record.

However, Examiner notes that such newly added limitation or approach is part of a design standard as described in IEEE 1149.1, as mentioned by Applicants' application on page 9 line 4. **Attaway et al.** (US Patent No. **5,701,308**; 23 Dec. 1997) incorporates such design approach for a built-in self-testing BIST architecture incorporating therein device under test and testing system, as follows.

Claim Objections

3. **Claim 16 is** objected to because the last line 2 should read "the at least **one** processor" instead of "the at least processor."

Claim Rejections - 35 USC § 112

4. The following is a quotation of the **second** paragraph of 35 U.S.C. 112:

> 2. The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4.1 Claims 1-5 and 18 are rejected under the **second paragraph of 35 U.S.C. 112** for failing to particularly point out and distinctly claim the subject matter which the applicant regards as his invention.

As per Claim 1 and **intervening claims**: It is not clear **to the Examiner** how the apparatus is operatively connected to effect testing of said apparatus. For example:

It is not seen how the control signal generation by the deskew controllers and the integrated test controller (ITC) synchronize to effect the testing operation.

It is not seen how the internal test bus (ITB) is controlled to allow the ITC to send test instructions to such ITB so as to shuttle such test instructions from the instrument register via such ITB to the logic unit controller.

It is not seen how the debug unit and the logic unit controller are coupled to effect the testing of said apparatus.

It is not seen how stimuli are applied to said apparatus or compare logic receives apparatus responses in testing said apparatus. It is assumed that a portion of said apparatus is tested.

4.1.1 As per Claims 3, 18, It is not clear to the Examiner how the signal distribution with 1st and 2nd local control signals is provided for ICs. The signal combination is ambiguous.

Claim Rejections - 35 USC ' 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

5.1 **Claims 1-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Wasson** (US Patent No. 6,181,151; Oct. 28, 1998 (filing date)) in view of **Attaway et al.** (US Patent No. 5,701,308; 23 Dec. 1997).

As per Claims 1, 6, 11, 16, Wasson substantially depicts, in Figs. 1-2 and related description in col. 1 line 10 et seq., the claimed apparatus or system or means circuit comprising: internal data bus (col. 2 line 55, or Fig. 1 numeral 24); plural clusters coupled to said bus with data signal synchronizing means for data signals there-through (Fig. 1 CH1..CHN); test controller coupled to said bus (col. 4 line 45 or col. 6 line 50 et seq., as seen in Fig. 1 Blocks 16 and 18); and a debug or tester or tester unit coupled to said bus (col. 4 line 47 et seq.) wherein the bus is configured to generate system or global control signal (at col. 4 lines 46 et seq.) and each of said plural clusters configured to generate local or separate control signals at col. 4 lines 49 et seq., wherein an IC embeds said ITC, clock controller means and entire tester components within a monolithic integrated circuit, e.g., in Fig. 1 and col. 3 line 45.

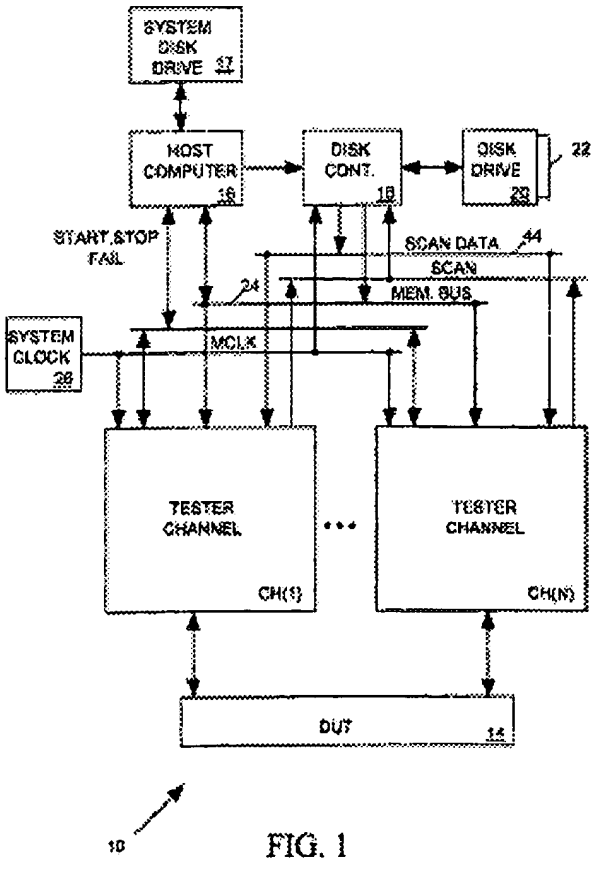

FIG. 1

Not specifically described in detail by **Wasson** is the step whereby the ITC has an instruction register and a test access port finite state machine and the tester is embedded along with the device under test in an IC.

However, **Examiner** notes that such **ITC** comprising an instruction register and a test access port finite state machine is part of a design standard as described in IEEE 1149.1, as conceded by Applicants' instant application on page 9 line 4. **Examiner** also notes that **Wasson** teaches the use of a finite state machine in Fig. 2 and memory means to store test instructions in plural channels in, e.g., col. 7 line 4.

Accordingly, such ITC so configured is well known as being part of an integrated circuit, said IC having a self-test feature. It is also is well known that some ICs comprise built-in self-testing (BIST) capabilities thereby **obviating the need for a bulky/expensive external tester and costly maintenance associated therewith**. For instance, **Attaway et al.** incorporates such design approach for a BIST system as depicted in Fig. 4 wherein *interface 10* comprises a *finite state machine 50* and *an instruction register 52*. {See **Attaway et al.**, Id., e.g., col. 3 line 25 for IEEE 1149.1 standard, col. 5 lines 34 for TAP finite state machine, col. 4 line 39 for instruction register, and RAM and *RAM BIST 40.*}

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the IC tester of **Wasson** by including therein TAP state machine and instruction register with a BIST system as taught by **Attaway et al.,** because such modification would provide the testing procedure of **Wasson** with a method whereby the testing system not only complies with the IEEE 1149.1 standard but also is cost efficient because such design minimizes test hardware overhead and eliminates operator intervention in test mode. {See **Attaway et al,** Id., Fig. 4: block 10.}

As per Claims 2, 17, Wasson depicts, in Fig. 2 and related description in col. 4 line 55 et seq., the claimed timing or sync or deskew buffer or memory means (Fig. 2 timing circuit 36) along with local clock driving means effected by Fig. 2 formatting circuit 38 as described in col. 5 line 27 et seq.

As per Claims 3, 7, 12, 18, Wasson depicts, in Fig. 2 and related description in col. 5 line 27 et seq., equivalent test control distribution means.

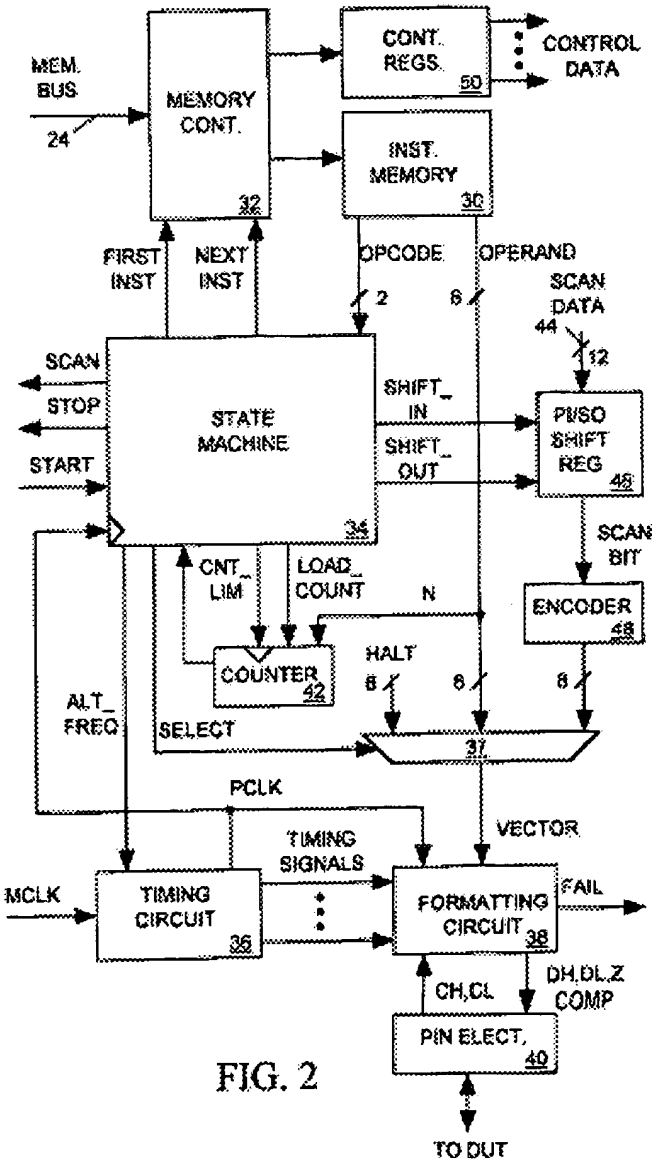

FIG. 2

As per Claims 4, 8, 13, 19, Wasson depicts, in Fig. 2 and related description in col. 5 line 27 et seq., equivalent snapshot instruction and shift instruction means, e.g., in Fig. 2 block 46 and col. 6 line 2-3, 43 et seq.

As per Claims 5, 9, 14, 20, Wasson depicts, in Fig. 2 and related description in col. 5 line 27 et seq., equivalent snapshot instruction and shift instruction means, e.g., in Fig. 2 block 46 and col. 6 line 2-3, 43 et seq.

As per Claim 10, 15, Wasson depicts, in Fig. 2 and related description in col. 6 line 62 et seq., the claimed debug or test triggering means via variable time period under control of state machine 34 of Fig. 2.

REMARKS

6.0 In response to Claims **1-20,** Applicants argue, on page 9, that the prior art of record does not teach the claims as amended.

Examiner notes that **Wasson** and **Attaway et al. render** Claims **1-20 obvious**.

Conclusion

6.1 The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6.2 Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6.3 Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 872-9306 for formal communications.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (703) 305-0755. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached on (703) 305-9595.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Guy J. Lamarre

Guy J. Lamarre, P.E
Patent Examiner
1/28/04